Applicant(s)	Frankie F. Roohparvar	**AMENDMENT AND RESPONSE**
Serial No.	09/608,580	
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Group Art Unit	2818	
Examiner Name	Trong Q. Phan	
Attorney Docket No.	400.006US01	
Title: ZERO LATENCY-ZERO BUS TURNAROUND SYNCHRONOUS FLASH MEMORY		

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G. Study
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AMENDMENT AND RESPONSE

Commissioner for Patents
BOX RCE
Washington, D.C. 20231

Prior to examination, please amend the application as follows:

IN THE CLAIMS

Please amend the claims as rewritten below:

C1

16. The synchronous memory device of claim 15 wherein the memory array is arranged in a plurality of memory blocks, and the control circuitry is configured to copy the data from the write latch to a first block of the plurality of memory blocks.

C4

25. The memory system of claim 24 wherein the memory array is arranged in a plurality of memory blocks, and the synchronous memory comprises control circuitry configured to copy the data from the write latch to a first block of the plurality of memory blocks.